[54] CMOS DATA INPUT-OUTPUT CIRCUIT

[75] Inventors: Hiroshi Yokouchi; Kazuhiko Miyazaki, both of Tokyo, Japan

[73] Assignee: Oki Electric Industry Co., Ltd., Tokyo, Japan

[21] Appl. No.: 739,304

[22] Filed: May 29, 1985

[30] Foreign Application Priority Data

May 30, 1984 [JP] Japan 59-108475

[51] Int. Cl.⁴ H03K 17/56; H03K 19/096; H03K 19/00

[52] U.S. Cl. 307/579; 307/242; 307/452; 307/473; 365/189

[58] Field of Search 307/451, 452, 473, 480, 307/481, 239, 242, 585, 579; 365/189, 233

[56] References Cited

U.S. PATENT DOCUMENTS

4,063,225 12/1977 Stewart 307/473
4,479,067 10/1984 Fujita 307/448

FOREIGN PATENT DOCUMENTS

0110774 8/1979 Japan 307/473

OTHER PUBLICATIONS

"Microcontroller Handbook", Design Considerations When Using CHMOS, Chapter 10, Issued by INTEL 1983, (Refer to pp. 10-1 and 10-2).

Primary Examiner—Stanley D. Miller
Assistant Examiner—M. P. Wambach
Attorney, Agent, or Firm—Wenderoth, Lind & Ponack

[57] ABSTRACT

In a CMOS type input-output circuit having an input control circuit, an output control circuit, a buffer circuit, a CMOS output buffer circuit and an input buffer circuit, the input-output circuit being capable of bidirectional transmission of information between a data bus and an I/O port, improvements on the control circuit are embodied by selecting a gate circuit in the input control circuit corresponding to that in the output control circuit. The output control circuit is connected to the input control circuit and the CMOS output buffer circuit. The CMOS output buffer circuit is connected to the input control circuit and the I/O port. Upon inputting a signal to both control circuits, the output control circuit causes the CMOS output buffer circuit to be electrically floating; the input control circuit outputs a level fixing signal regardless of the logic level of the I/O port.

6 Claims, 8 Drawing Figures